Design considerations bring unity to a mixed-voltage world

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If you design with low-voltage devices, you've probably encountered the compatibility issue of making systems operate with some 5V devices. A few design considerations, such as how to mix voltages, might bring your system into harmony.

The market for low-voltage (3.3V and below) systems is growing. One factor fueling this growth is the emphasis on protecting the environment: To save energy, "green" machines operate at lower voltages than do traditional devices. Technology is another driving force in the market. As IC technology advances, transistor geometries are decreasing to submicron sizes that cannot handle standard 5V voltages.

However, not every IC manufacturer has entered the still-emerging market for low-voltage devices. Until all manufacturers make the switch to low voltages, designers must take precautions to ensure proper operation of mixed 3/5V hybrids.

Currently, 3V devices dominate the markets for mobile computing and communications. This market comprises portable PCs, including notebook and subnotebook computers, and personal information devices, including handheld computers and electronic books. Mobile-communication products include cellular phones, pagers, and other personal communicators. Although the major thrust of 3V devices is for portable systems, desktop systems can still reap the advantages of lower voltages.

To succeed in the market for portable computing and communications, systems must offer low size and weight; energy efficiency for extended operating life; performance rivaling full-power systems but maintaining low-power systems' cost-effectiveness; user-friendly interfaces, such as voice, pen, and touch inputs; wireless-communications capability; ruggedness; and dependability.

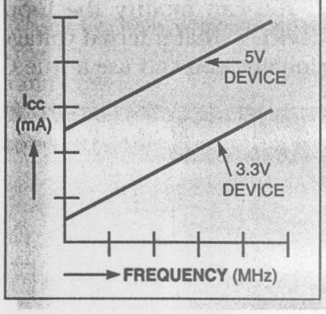
Power in hybrid designs is directly proportional to the square of the supply voltage. Thus, switching from a 5 to a 3V supply yields a 44% reduction in power, as the following equations show:

$$P_{3.3}=V^2/R=(3.3)^2/R=10.89/R$$
$$P_5=V^2/R=(5)^2/R=25/R$$
$$P_{3.3}/P_5=0.44=44\%,$$

where P=power, V=supply voltage, and R=resistance.

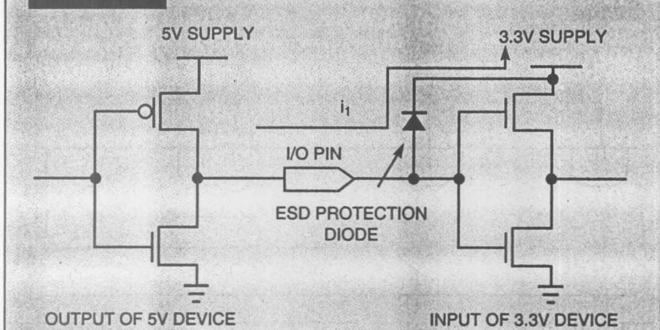
Because power, voltage, and current affect each other, the current decreases as the voltage decreases (Fig 1). For example, a 5V version of a 33-MHz Intel 486DX μP operating offers a 900-mA current rating, and a 3V version of a 33-MHz

FIGURE 1



Because power, voltage, and current affect each other, the current decreases as the voltage decreases, which contributes to a 44% power savings.

FIGURE 2



A 5V CMOS device driving a 3.3V CMOS device might forward-bias the ESD protection diode and cause excessive current.

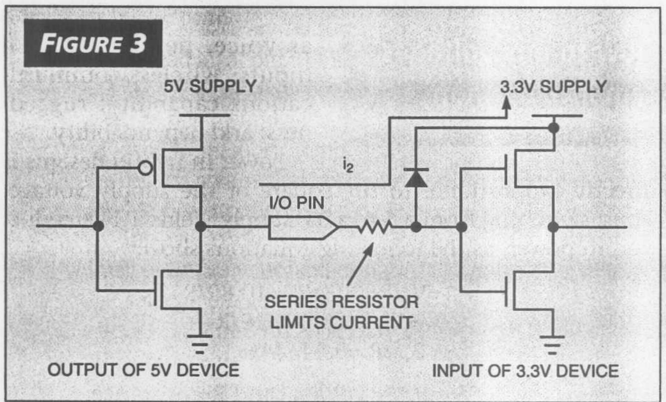
Advanced Micro Devices 486DX µP offers a 425-mA current rating. Switching to a 3V design causes the current requirements to drop by more than half. Because there are no major developments in battery technology, designers must build systems that run longer on existing power supplies. The lower voltage technology will help designers achieve that goal.

Lower voltages yield many benefits

Because the systems requires only 3.3V, unregulated power supplies, such as standard alkaline batteries, are sufficient to operate a system. Because systems no longer require large regulated power supplies, system form factors and weights also decrease, which is important in handheld and portable systems.

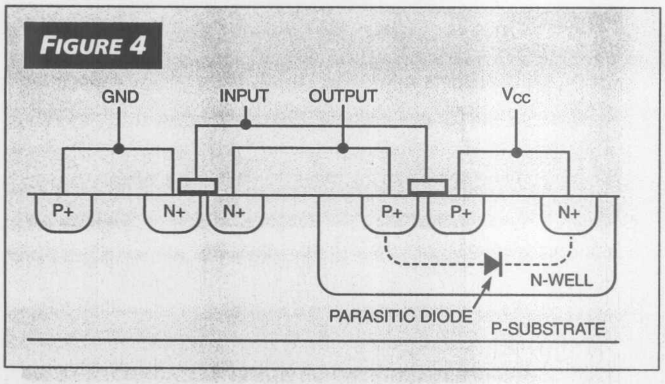
Switching to a 3V supply also reduces the output-voltage swings, making the systems produce less noise. The lower voltages also reduce EMI emissions and make them easier to control; as a result, standard-setting institutions, such as the FCC, will be more likely to approve 3V systems. In addition, 3V systems inevitably run cooler than 5V systems, leading to increased system reliability.

FIGURE 3



If board space is critical but speed is not, place a series resistor between the 3 an 5V devices to limit the current flowing from the 5V device into the 3V device.

FIGURE 4



Internally alter the the source and drain region of a true CMOS device to eliminate the parasitic diode, thus eliminating excessive current draw.

Pay careful attention to device placement and usage in a hybrid design. The following guidelines apply to a design that integrates 3.3 and 5V devices. Interfacing 3V TTL devices to 5V TTL devices typically causes no problem because the 3V TTL-device outputs have the same characteristics as those of the 5V TTL-device outputs.

Interfacing 3V TTL or CMOS devices to 5V CMOS devices, however, causes problems because the 5V devices need extra drive to prevent leakage current. Many voltage translation devices, such as Performance Semiconductor's PCT3 voltage translation series, translate from 3.3 to 5V. However, this solution adds delay and board space.

Interfacing 3V CMOS devices to 5V TTL devices doesn't compromise performance because the 3V device outputs have sufficient margin to drive 5V TTL-device inputs. However, you cannot directly connect a 5V output to a 3V input. Driving a 3V input, a 5V output can exceed the maximum supply-voltage rating and can forward-bias the ESD protection diode. The diode allows excess current to flow from the 5V device into the 3V power supply, possibly inducing latch-up (**Fig 2**). In this case, use voltage-translation devices.

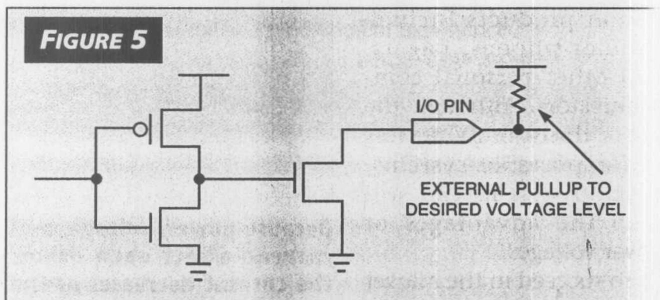
Space-vs-speed trade-offs

If board space is critical but speed is not, you can place a series resistor between the 3 and 5V devices to limit the current flowing from the 5V device into the 3V device (**Fig 3**). The series resistor makes **Fig 3's** i_2 less than **Fig 2's** i_1. However, if speed is critical, you should consider another method because adding a series resistor increases the device's propagation delay. Further, adding components increases board space and reduces noise immunity and system reliability.

Plan carefully when designing a system that requires devices of different voltages to reside on the same bus. In the previous scenarios, voltage translations were unidirectional, but a bus application requires bidirectional interfaces. One such interface, the Integrated Device Technology 74FCT164245, provides bidirectional 3-to-5V translation, with 3 or 5V signals driving the control inputs. Regardless of whether a 3V device resides on a 5V bus or a 5V device resides on a 3V bus, run the bus at one voltage and use translation circuitry and buffers between the other devices.

You can modify the input and output structures of a device so that internal voltage translations can occur. Occasionally, you can use a true CMOS transmission gate at the

FIGURE 5



Place an external pull-up resistor in the open-drain output of a CMOS device to accomplish the voltage translation.

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output. A parasitic diode exists between the source/drain region and the diffusion well (**Fig 4**). If a 5V signal drives the I/O pin, the parasitic diode forward-biases and produces a path for current. By modifying the output structure to omit the pnp transistor, the input can now rise above 3.3V. Adding a transistor to an output structure prevents output latch-up, solving the problems that external translation circuitry cause.

Derating a 5V device for use as a 3V device may cause insufficient drive capability. The 3V devices operate at lower supply voltages, lowering the devices' output-drive capabilities. If you want to use these devices in bus applications, determine whether the parts are derated or truly low-voltage devices: A derated part often offers lower performance than that of an equivalent 5V device, whereas a true low-voltage design performs as well as or better than its 5V counterpart.

Another possibility for interfacing 5 and 3V devices is to use a device, such as Advanced Micro Devices' PALCE16V8HD, with an open-drain-output configuration. These devices act as buffers and ensure safe operation of 3.3V devices. However, a device with an open-drain option may have an internal pull-up transistor whose parasitic diode may forward-bias, causing current to flow. A true open-drain device requires only an external pull-up resistor to the desired voltage level (**Fig 5**).

Hybrid systems include multiple voltage supplies, so you must prevent latch-up on the I/Os during power-up and -down. To prevent latch-up on power-up, make sure that the 5V supply is greater than or equal to the 3V supply. To prevent latch-up on power-down, the 3V supply should be less than or equal to the 5V supply. Many chip sets, such as Pico Power's Evergreen HV PT86C268, run on dual power supplies and provide control signals for peripheral and system power planes. To take full advantage of the two voltage devices, mix the design on the board so that the speed-critical paths run at 5V and the low-power paths run at 3.3V.

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Author's biography

Kenneth M Cuy is an applications engineer at Advanced Micro Devices' Programmable Logic Division in Sunnyvale, CA, where he has worked for three years. In his current position, he provides applications support for Mach 3 and 4 devices. He has also helped develop CMOS PLDs, such as the 16V8, 20V8, and 22V10, and high-density Mach 1, 2, 3, and 4 devices. Cuy has a BSEE from Rensselaer Polytechnic Institute (Troy, NY), and lists photography and mountain biking as his hobbies.

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